

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

GARG *et al.*

Appl. No.: 10/060,086

Filed: January 31, 2002

For: **RISC Microprocessor Architecture
Implementing Multiple Typed
Register Sets**

Confirmation No.: 6414

Art Unit: 2154

Examiner: Larry D. Donaghue

Atty. Docket: 2047.0600007

Fifth Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms PTO/SB/08A and PTO/SB/08B are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

In addition, Applicants hereby inform the Examiner of current litigation involving parent patents to which the present application claims priority. This disclosure is being made in accordance with MPEP 2001.06(c). The relevant litigation is *Transmeta Corporation v. Intel Corporation*, 1:06-cv-00633-GMS, U.S. District Court of Delaware. The litigation involves U.S. Pat. No. 5,493,687, issued February 20, 1996, U.S. Pat. No. 5,838,986, issued November 17, 1998, and U.S. Pat. No. 6,044,449, issued March 28, 2000, which are all part of the priority chain of the present application. Documents NPL1-NPL3 on the attached Form PTO/SB/08B are documents related to this litigation. As they become available, Applicants will provide the Examiner with additional documents from the litigation that are material to the patentability of the

present application in accordance with *Critikon, Inc. v. Becton Dickinson Vascular Access, Inc.*, 120 F.3d 1253 (Fed. Cir. 1997).

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached IDS Forms PTO/SB/08A and PTO/SB/08B based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed concurrently with the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

Copies of documents NPL1-NPL17 are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), copies of the U.S. patents cited on the attached Form PTO/SB/08A are not submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application nos. 09/840,026, filed April 24, 2001 (now abandoned), 09/480,136, filed January 10, 2000 (now Pat. No. 6,249,856), 09/188,708, filed November 10, 1998 (now Pat. No. 6,044,449), 08/937,361, filed September 25, 1997 (now Pat. No. 5,838,986), 08/665,845, filed June 19, 1996 (now Pat. No. 5,682,546), 08/465,239, filed June 5, 1995 (now Pat. No. 5,560,035), and 07/726,773, filed July 8, 1991 (now Pat. No. 5,493,687), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution histories has been reviewed in connection with the present application.

The Examiner's attention is also directed to the prosecution history and cited art in application no. 11/651,009, filed January 9, 2007, which claims priority to the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms PTO/SB/08A and PTO/SB/08B, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read "Donald J. Featherstone", written over the printed name.

Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

Date: June 6, 2007

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Substitute for form 1449/PTO				Complete if Known	
FIFTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	10/060,086
				Filing Date	January 31, 2002
				First Named Inventor	Sanjiv GARG
				Art Unit	2154
				Examiner Name	Larry D. Donaghue
Sheet	1	of	1	Attorney Docket Number	2047.0600007

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if Known)			
	US1	5,179,689	01-12-1993	Leach <i>et al.</i>	
	US2	5,249,286	09-28-1993	Alpert <i>et al.</i>	
	US3	4,980,817	12-25-1990	Fossum <i>et al.</i>	
	US4				
	US5				
	US6				
	US7				
	US8				
	US9				
	US10				
	US11				
	US12				
	US13				
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	US15				
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	US17				
	US18				
	US19				
	US20				

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP7					
	FP8					
	FP9					

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet	1	of	2	Attorney Docket Number	2047.0600007

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	<i>Complaint</i> , 7 pages, filed October 11, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL2	<i>First Amended Complaint</i> , 7 pages, filed December 12, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL3	<i>Intel Corporation's Answer, Affirmative Defenses, and Counterclaims to Transmeta's First Amended Complaint</i> , 27 pages, filed January 9, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL4	G. Myers <i>et al.</i> , <i>The 80960 Microprocessor Architecture</i> , John Wiley & Sons, Inc., 1988.	
	NPL5	<i>Third-Generation TMS320 User's Guide</i> , Texas Instruments, 1988.	
	NPL6	<i>Convex Architecture Handbook, Version 1</i> , Convex Computer Corporation, 1984.	
	NPL7	Butler, M. <i>et al.</i> , "Single Instruction Stream Parallelism Is Greater than Two," <i>Proceedings of the 18th Annual International Symposium on Computer Architecture</i> , ACM, pp. 276-286 (May 1991).	
	NPL8	Hennessey, J.L. and Patterson, D.A., <i>Computer Architecture: A Quantitative Approach</i> , Morgan Kaufmann Publishers, pp. xi-xv, 257-278, 290-314 and 449 (1990).	
	NPL9	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).	
	NPL10	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," <i>Conference Proceedings: 1988 International Conference on Supercomputing</i> , ICS, July 4-8, 1988, pp. 346-353.	

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.
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	NPL11	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 1990).	
	NPL12	Hwu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," <i>Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences</i> , pp. 330-336 (1987).	
	NPL13	Hwu, W-M. et al., "An HPS Implementation of VAX: Initial Design and Analysis," <i>Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences</i> , pp. 282-291 (1986).	
	NPL14	Hwu, W. and Patt, Y., "HPSm2: A Refined Single-Chip Microengine," <i>HICSS '88</i> , IEEE, pp. 30-40 (1988).	
	NPL15	Patt, Y.N. et al., "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," <i>COMPCON 86</i> , IEEE, pp. 254-258 (1986).	
	NPL16	Patt et al., "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," <i>Proceedings of MICRO 19 Workshop</i> , New York, pp. 75-81 (October 1986).	
	NPL17	Wilson, J.E. et al., "On Tuning the Microarchitecture of an HPS Implementation of the VAX," <i>Proceedings of the 20th Annual Workshop on Microprogramming</i> , IEEE Computer Society, pp. 162-167 (December 1-4, 1987).	
	NPL18		
	NPL19		
	NPL20		

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